Notice of Allowability	Application No.	Applicant(s)	
	10/630,647	BECK ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed 9/20/2007 and interview on 12/19/2007*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/11/2007 and 9/20/2007 has been entered.

Response to Arguments

2. Applicant's arguments, filed 9/20/2007, with respect to claims 1-19 and new claim 20 have been fully considered and are persuasive (in condition with additional amendments for clarification as set forth below in the Examiner's amendment section). The rejection of claims 1-19 has been withdrawn.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with **Jack J. Jankovitz** (Reg. No. 42,690) on 12/19/2007.

The application has been amended as follows:

In the claims:

(Please note that amendments are shown in underline, strikethrough and/or double square brackets)

Claim 1 (Currently Amended) A pixel-capture circuit, comprising:

a pixel-capture device having a pixel node and operable to convert light intensity into a pixel signal at the pixel node, the pixel signal representing a captured pixel;

a row node directly connected to a gate of a row selection transistor for carrying a row signal that is operable to couple the pixel node to a column trace during a read period of the captured pixel and operable to set the pixel node to a predetermined signal level during a reset period; and

a reset node carrying a reset signal that is operable to directly couple the row node to the pixel node during the reset period,

wherein the row signal changes between predetermined voltage levels during at least one portion of the reset period and sets the pixel node to the predetermined signal level such that the row node is coupled to the pixel node during the reset period.

Claim 9 (Currently Amended) A pixel-capture circuit, comprising:

a pixel-capture device having a first node and a second node, the first node coupled to a first supply node;

a first transistor having a control node, a first drive node, and a second drive node, the control node directly connected to the second node of the pixel-capture device and the first drive node coupled to a second supply node;

a second transistor having a control node, a first drive node, and a second drive node, the control node of the second transistor connected to a row node, the first drive node of the second transistor connected to the second drive node of the first transistor, the second drive node of the second transistor directly connected to a column node; and

a third transistor having a control node, a first drive node, and a second drive node, the control node of the third transistor coupled to a reset node, the first drive node of the third transistor directly connected to the row node, the second drive node of the third transistor directly connected to the second node of the of the pixel-capture device,

wherein the row node carries a row signal, the row signal changes between predetermined levels during at least one portion of a reset period.

Claim 11 (Currently Amended) A CMOS array comprising:

a plurality of pixel-capture circuits arranged in rows and columns, each pixel-capture circuit comprising:

a pixel-capture device having a pixel node and operable to convert light intensity into a pixel signal at the node, the pixel signal representing a captured pixel;

a row node directly connected to a gate of a row selection transistor for carrying a row signal that is operable to couple the pixel node to a column trace during a read period of the captured pixel and operable to set the node to a predetermined signal level during a reset period; and

a reset node carrying a reset signal that is operable to directly couple the row node to the pixel node during the reset period,

wherein the row signal changes between predetermined levels during at least one portion of the reset period and sets the pixel node to the predetermined signal level during the reset period such that the row node is coupled to the pixel node during the reset period.

Claim 14 (Currently Amended) A system comprising:

a CMOS array having:

a plurality of pixel-capture circuits arranged in rows and columns, each pixel-capture circuit comprising:

a pixel-capture device having a pixel node and operable to convert light intensity into a pixel signal at the pixel node, the pixel signal representing a captured pixel; and

a row node directly connected to a gate of a row selection transistor for carrying a row signal that is operable to couple the pixel node to a column trace during a read period of the captured pixel and operable to

set the pixel node to a predetermined signal level during a reset period; and

a reset node carrying a reset signal that is operable to directly couple the row node to the pixel node during the reset period,

a processor coupled with the CMOS array and operable to facilitate detection of a voltage signal at each column trace in each pixel in the CMOS array,

wherein the row signal changes between predetermined levels during at least one portion of the reset period and sets the pixel node to the predetermined signal level such that the row node is coupled to the pixel node during the reset period.

Claim 16 (Currently Amended) A method[[,]] comprising the steps of:

integrating an amount of light;

generating a light level signal on a pixel node, the pixel node signal having a level related to the integrated amount of light;

generating a first control signal on a first control node which is directly connected to a gate of a row selection transistor;

generating a second control signal on a second control node to control resetting of the light level signal;

reading the light level signal in response to the control signal on the first control node; and

resetting a level of the light level signal at the pixel node in response to the second control signal, wherein the resetting of the level of the light level signal ~~level~~ occurs during a reset period and includes connecting the first control node directly to the pixel node via a switching device in response to the second control signal and driving the resetting of the level of the light level signal using the first control signal, the first control signal changing between predetermined levels during at least one portion of the reset period.

Claim 18 (Currently Amended) The method of claim 16 wherein the driving of the resetting of the level of the light level signal comprises:

setting a level at the another control node to a predetermined high level; and

pulsing ~~the~~ a level at the first control node to a predetermined low level from the predetermined high level, the predetermined high level being higher than the predetermined low level.

Claim 19 (Currently Amended) The circuit of claim 1, further comprising:

a reset transistor for controlling reset of the pixel signal at the pixel node of the [[pixel capture]] pixel-capture device, the reset transistor being controlled by the reset signal from the reset node, the reset transistor connecting the row signal to the pixel node during the reset period and disconnecting the row signal from the pixel node during ~~the~~ an image-capture period; ~~and~~

~~a row-selection transistor,~~

wherein the row node is coupled to the reset transistor to selectively couple the row node to the pixel node of the [[pixel capture]] pixel-capture device for reset and the row node is further coupled to the row selection transistor to control the row selection transistor to selectively couple the pixel node of the [[pixel capture]] pixel-capture device to the column trace for readout.

Claim 20 (Currently Amended) The circuit of claim 19, wherein:

the row selection transistor couples the pixel node of the [[pixel capture]] pixel-capture device to the column trace during the readout period and uncouples the pixel node from the column trace during the image-capture period; and

a further transistor connected between the [[pixel capture]] pixel-capture device and the row selection transistor, the row selection transistor being disposed between the further transistor and the column trace.

Allowable Subject Matter

4. Claims 1-20 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Regarding claims 1 and 11, the prior art of record fails to teach or fairly suggest the combination of all limitations of each of claims 1 and 11 that includes **"a reset node carrying a reset signal that is operable to directly couple the row node to the pixel node during the reset period, wherein the row signal changes between predetermined voltage levels during at least one portion of the reset period and**

sets the pixel node to the predetermined signal level such that the row node is coupled to the pixel node during the reset period."

Regarding claim 14, this claim is allowed for the same reason as cited in claims 1 and 11 above.

Regarding claim 9, the prior art of record also fails to teach or fairly suggest the combination of all limitations of claim 9 that includes **"a second transistor having a control node, a first drive node, and a second drive node, the control node of the second transistor connected to a row node, the first drive node of the second transistor connected to the second drive node of the first transistor, the second drive node of the second transistor directly connected to a column node; and a third transistor having a control node, a first drive node, and a second drive node, the control node of the third transistor coupled to a reset node, the first drive node of the third transistor directly connected to the row node, the second drive node of the third transistor directly connected to the second node of the of the pixel-capture device, wherein the row node carries a row signal, the row signal changes between predetermined levels during at least one portion of a reset period."**

Regarding claim 16, the prior art of record also fails to teach or fairly suggest the combination of all limitations of claim 16 that includes **"resetting a level of the light level signal at the pixel node in response to the second control signal, wherein the resetting of the level of the light level signal occurs during a reset period and includes connecting the first control node directly to the pixel node via a**

switching device in response to the second control signal and driving the resetting of the level of the light level signal using the first control signal, the first control signal changing between predetermined levels during at least one portion of the reset period."

Regarding claims 2-8, 19 & 20, these claims are allowed as being directly or indirectly dependent from claim 1.

Regarding claim 10, this claim is allowed as being dependent from claim 9.

Regarding claims 12 & 13, these claims are allowed as being directly or indirectly dependent from claim 11.

Regarding claim 15, this claim is allowed as being dependent from claim 14.

Regarding claims 17 & 18, these claims are allowed as being dependent from claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner